RISC-V Processor

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Introduction

The aim of this project is to build an SoC (System on Chip) with a 32-bit extended RISC-V core with custom instructions for specialized use cases for cryptography and neural networking purposes on an FPGA.

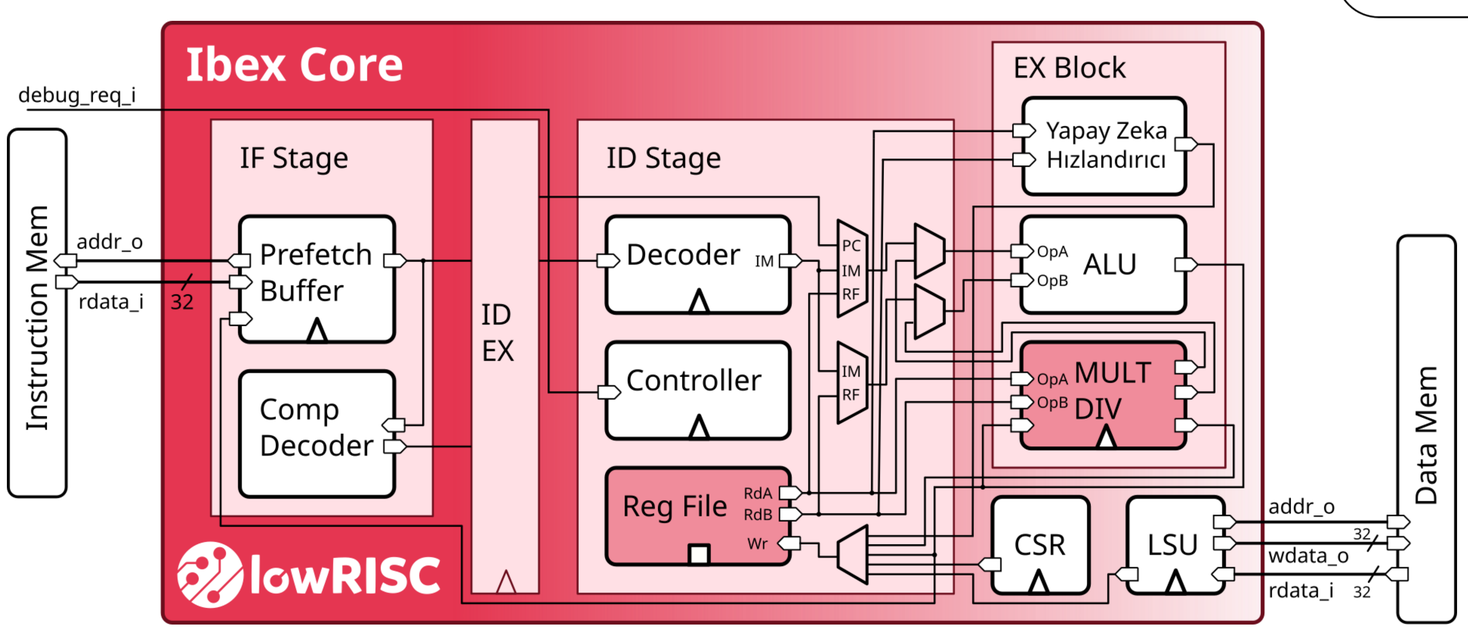
The SoC supports RISC-V RV32IMCX instructions and has two caches for fast memory access for data and instructions. Also, an AI accelerator module is included for use for fast 2D convolution calculations.

This SoC is built with competing in the Teknofest chip design competition in mind. Furthermore, the project reached the finals of this year's competition and can be further developed within the next 1 to 2 years with the aim of winning the competition.

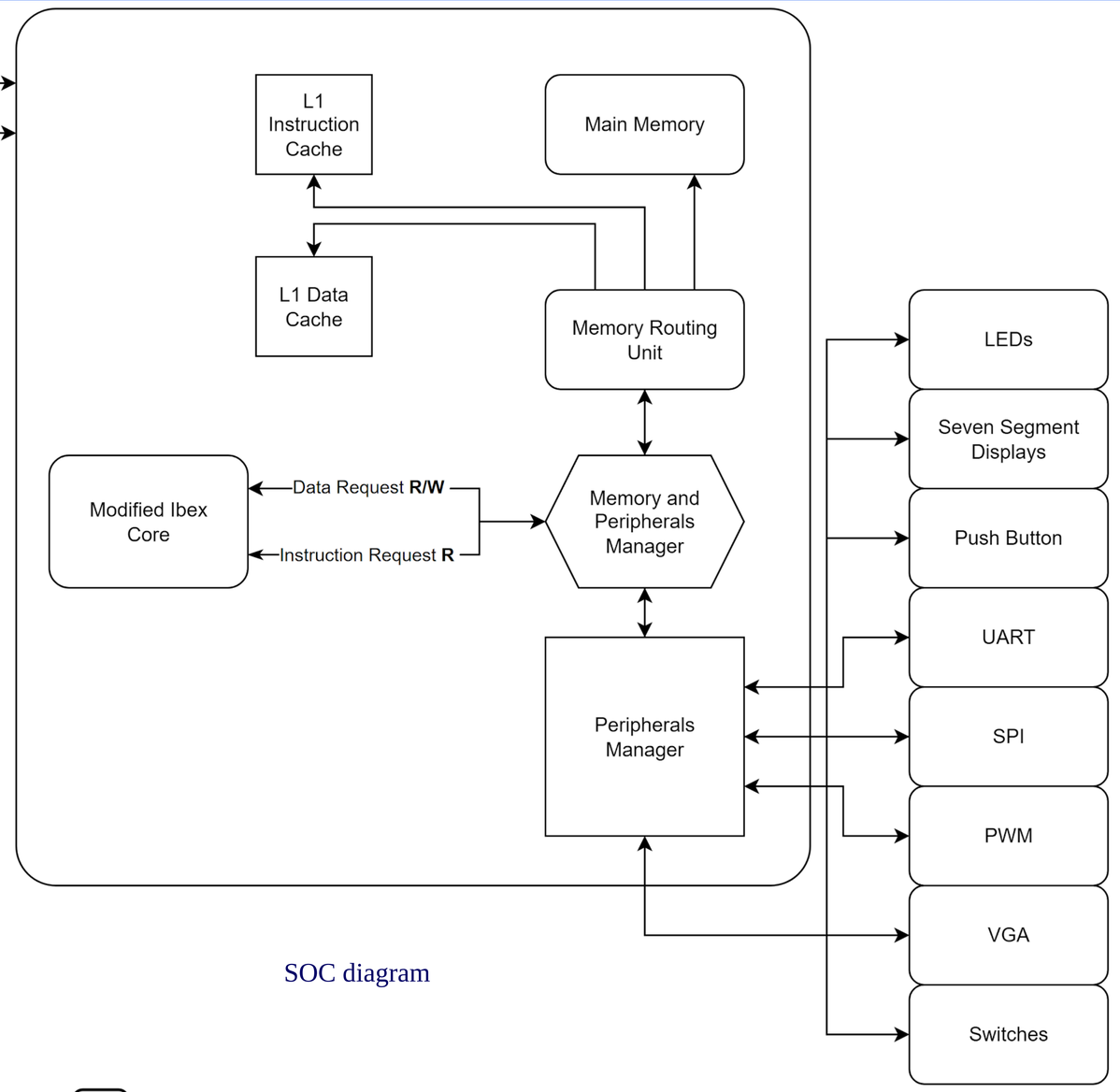
Overview

The objective of this project is to develop a System-on-a-Chip (SoC) that houses a 32-bit RISC-V CPU and supports the RISC-V standard extensions RV32IMC and an extra 11 additional custom non-standard instructions for specialized use cases in cryptography and neural networking. The project comes at a time of pushing towards open-source hardware and embodies the idea by building an SoC using an open-source CPU core that runs an open-source ISA. The SoC also houses main memory and L1 cache elements as well as a VGA module and basic SPI, PWM, and UART transmission peripherals.

Results



Core diagram



SOC diagram

Conclusions

Should the DE10-lite FPGA be used in future studies, it is important to be able to utilize the 64MB SDRAM chip on the FPGA board. Even if the development will continue with different FPGA boards, it would be beneficial to be able to utilize the SDRAM chip on said chip.
The Teknofest competition is said to continue running in the next few years where the competition specifications will not see major changes. And since the current form of the project is compatible with the specifications but needs further developments, setting the Teknofest competition as the goal for future works is viable.

References

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